SCALABLE SERIALIZER-DESERIALIZER ARCHITECTURE AND PROGRAMMABLE INTERFACE

ABSTRACT

Systems and methods are disclosed to provide programmable input/output functionality for a programmable logic device. For example, in accordance with one embodiment of the present invention, a programmable interface selectively employs a scalable serializer-deserializer and clock and data recovery circuit. The programmable interface further includes programmable input/output buffers and embedded memory to allow the programmable logic device to support a wide range of input/output interface standards.